Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Canceled)

2. (Canceled)

3. (Previously Presented) The apparatus as claimed in claim 11, wherein uncompressed digital video streams having been edited are transferred from said video output of said graphics accelerator chip to said codec for compression and storage in said storage device.

4. (Previously Presented) The apparatus as claimed in claim 3, wherein said graphics accelerator chip has an input buffer for storing a sequence of fields of said at least two real-time uncompressed digital video streams and an output buffer for storing a sequence of fields of said uncompressed digital video streams having been edited.

5. (Original) The apparatus as claimed in claim 4, wherein said input buffer also stores input graphic image fields.

6. (Previously Presented) The apparatus as claimed in claim 11, wherein said graphics accelerator chip has an input buffer for storing a sequence of fields of said at least two real-time uncompressed digital video streams and an output buffer for storing a sequence of fields of said uncompressed digital video streams having been edited.

7. (Original) The apparatus as claimed in claim 6, wherein said input buffer also stores input graphic image fields.

8. (Canceled)

9. (Previously Presented) The apparatus as claimed in claim 7, further comprising an input for compressed digital video streams from an external device, and a decompression device, one of said at least two real-time uncompressed digital video streams comprising decompressed data from said compressed digital video stream.

10. (Previously Presented) The apparatus as claimed in claim 9, wherein said input for compressed digital video streams comprises one of an IEEE 1394 interface and an SDTI interface.

11. (Currently Amended) A video editing apparatus for performing video editing in real-time of video streams, the apparatus comprising:

a video decoder for producing uncompressed digital video streams from said video streams;

a storage device for storing video data;

a codec for providing at least two real-time uncompressed digital video streams from at least one of said video data provided by said storage device and said uncompressed digital video streams provided by said video decoder;

a graphics accelerator chip having at least two video inputs for ~~respectively~~ receiving said at least two real-time uncompressed digital video streams, said graphics accelerator chip further having a 2D graphics engine and a 3D rendering engine respectively for providing 2D and 3D functions used for said video editing of said at least two real-time uncompressed digital video streams, said graphics accelerator chip further comprising a video output for providing edited uncompressed digital video streams;

a video encoder for providing a display signal from at least one of said uncompressed digital video streams and said edited uncompressed digital video streams;

a first video bus for transferring said uncompressed digital video streams from said video decoder to said codec, and for transferring said edited uncompressed digital video streams from said video output to said video encoder when said apparatus is operating in a real-time video editing mode; and

a time division multiplexed bus for transferring said at least two real-time uncompressed digital video streams from said codec to said at least two video inputs when said apparatus is operating in a real-time video editing mode.

12. (Previously Presented) The apparatus as claimed in claim 11, wherein said video decoder uses said first video bus for transferring uncompressed video digital video streams to said video encoder in a non-editing playback mode, and said video decoder uses said first video bus for transferring uncompressed digital video streams from said video decoder to said codec in a video capture mode.

13. (Previously Presented) The video editing apparatus of claim 11, wherein each of said at least two video inputs is coupled to said 3D rendering engine, and wherein said video output is coupled to said 3D rendering engine.

14. (Previously Presented) The video editing apparatus of claim 13, wherein each of said at least two video inputs is coupled to said 2D graphics engine, and wherein said video output is coupled to said 2D graphics engine.

15. (Previously Presented) A method of editing a plurality of video streams with a graphics accelerator chip that includes a 2D graphics engine and a 3D rendering engine, the method comprising acts of:

receiving a first real-time uncompressed digital video stream at a first input of the graphics accelerator chip;

receiving a second real-time uncompressed digital video stream at a second input of the graphics accelerator chip;

performing video editing on the first real-time uncompressed digital video stream and the second real-time uncompressed digital video stream using the 2D graphics engine and the 3D rendering engine; and

generating an edited uncompressed digital video stream at a video output of the graphics accelerator chip, wherein said edited uncompressed digital video stream includes edited video from at least one of the first real-time uncompressed digital video stream and the second real-time uncompressed video stream.

16. (Previously Presented) The method of claim 15, further comprising an act of mapping at least one of the first real-time uncompressed digital video stream and the second real-time uncompressed digital video stream onto a target surface.

17. (Previously Presented) The method of claim 15, further comprising an act of communicating the first real-time uncompressed digital video stream to a video input buffer included in the graphics accelerator chip.

18. (Previously Presented) The method of claim 15, wherein the first real-time uncompressed digital video stream originates from a video data storage medium.

19. (Previously Presented) The method of claim 15, further comprising an act of transferring the edited uncompressed digital video stream from the video output of the graphics accelerator chip to a storage device.

20. (Previously Presented) The method of claim 15, further comprising an act of receiving graphics data at a third input of the graphics accelerator chip.

21. (Previously Presented) The method of claim 20, further comprising an act of communicating the graphics data to an input buffer included in the graphics accelerator chip.

22. (Previously Presented) The method of claim 20, further comprising an act of communicating the graphics data to at least one of the 3D rendering engine and the 2D graphic engine.

23. (Previously Presented) The method of claim 17, further comprising acts of receiving graphics data at a third input of the graphics accelerator chip and communicating the graphics data to a graphics input buffer included in the graphics accelerator chip.

24. (Currently Amended) A video editing apparatus for performing video editing in real time, the apparatus comprising:

a graphics accelerator chip having at least two video inputs for ~~respectively~~ receiving at least two real-time uncompressed digital video streams, said graphics accelerator chip further having a 2D graphics engine and a 3D rendering engine respectively for providing 2D and 3D functions used for said video editing of said at least two real-time uncompressed digital video streams, said graphics accelerator chip further comprising a video output for providing edited uncompressed digital video streams.

25. (Previously Presented) The apparatus as claimed in claim 24, further comprising a codec and a storage device, wherein uncompressed digital video streams having been edited are transferred from said video output of said graphics accelerator chip to said codec for compression and storage in said storage device.

26. (Previously Presented) The apparatus as claimed in claim 24, wherein said graphics accelerator chip includes an input buffer for storing a sequence of fields of said at least two real-time uncompressed digital video streams and an output buffer for storing a sequence of fields of said uncompressed digital video streams having been edited.

27. (Previously Presented) The apparatus as claimed in claim 26, wherein said input buffer also stores input graphic image fields.

28. (Previously Presented) The apparatus as claimed in claim 27, further comprising an input for compressed digital video streams from an external device, and a decompression device, one of said at least two real time uncompressed digital streams comprising decompressed data from said compressed digital video stream.

29. (Previously Presented) The apparatus as claimed in claim 28, wherein said input for compressed digital video streams comprises one of an IEEE 1394 interface and an SDTI interface.

30. (New) A video editing apparatus for performing video editing in real time, the apparatus comprising:

a graphics accelerator chip including:

a plurality of video inputs including:

a first video input configured to receive a first real-time uncompressed digital video stream including a first plurality of video frames; and

a second video input configured to receive a second real-time uncompressed digital video stream including a second plurality of video frames;

a graphics input configured to receive graphics data;

a 2D graphics engine and a 3D rendering engine each coupled to the first video input, the second video input and the graphics input, the 2D graphics engine and the 3D graphics engine configured to provide 2D and 3D functions, respectively, and to perform video editing in real time of the first real-time uncompressed digital video stream and the second real-time uncompressed digital video stream to generate an edited uncompressed digital video stream that includes at least a portion of one video frame of the first plurality of video frames, at least a portion of one video frame of the second plurality of video frames and the graphics data; and

a video output configured to output the edited uncompressed digital video stream.

31. (New) The video editing apparatus of claim 30, wherein the graphics accelerator chip further includes a first input buffer coupled to the first video input, wherein the first video input is coupled to the 2D graphics engine and the 3D rendering engine via the first input buffer; and a second input buffer coupled to the second video input, wherein the second video input is coupled to the 2D graphics engine and the 3D rendering engine via the second input buffer.

32. (New) The video editing apparatus of claim 31, wherein the graphics accelerator chip further includes a graphics input buffer coupled to the graphics input, wherein the graphics input is coupled to the 2D graphics engine and the 3D rendering engine via the graphics input buffer.